CLAIMS:

1. A data processing system, comprising:
- a plurality of processing elements (COP1, COP2), which are arranged for synchronously processing data under control of at least one clock facility;
- at least one local controller (CTR1, CTR2) associated with a processing element of the plurality of processing elements;
- a data communication means (SB) arranged for exchanging data between processing elements of the plurality of processing elements,
wherein the local controller is arranged for powering down its associated processing element depending on the required processing capacity of that processing element.

2. A data processing system according to claim 1, wherein the local controller is further arranged for powering up its associated processing element depending on the required processing capacity of that processing element.

3. A data processing system according to claim 1, further comprising:
- at least one buffer (BI1, BI2) associated with the processing element of the plurality of processing elements, wherein the buffer is arranged for exchanging data between its associated processing element and the data communication means,
and wherein the local controller is arranged to determine the required processing capacity of its associated processing element from the filling degree of the associated buffer.

4. A data processing system according to claim 1, further comprising a control processor,
wherein the local controller is arranged to receive information on the required processing capacity of the associated processing element from the control processor,
and wherein the local controller is further arranged to have information on the processing capacity of the associated processing element.

5. A data processing system according to claim 1, wherein the processing element of the plurality of processing elements is further arranged to generate an interrupt for notifying its associated local controller on the required processing capacity.

6. A data processing system according to claim 1, wherein a sequence of clock cycles effects a processing operation of an amount of data,
wherein the data processing system further comprises programmable means for implementing programmable stall clock cycles for the processing element of the plurality of processing elements, wherein the programmable stall clock cycles are interspersed between clock cycles of the sequence of clock cycles.

7. A data processing system according to claim 1, wherein at least one processing element is associated with a bandwidth control unit (BCTR) for controlling a rate of its data transfer along the data communication means, the bandwidth control unit restricting the data transfer if it exceeds an allowed maximum data rate.

8. A data processing system according to claim 1, further comprising a memory facility (MEM),
wherein the data communication means is further arranged for exchanging data between the memory facility and the processing elements of the plurality of processing elements.

9. A method for processing data, using a data processing system, comprising:
- a plurality of processing elements (COP1, COP2), which are arranged for synchronously processing data under control of at least one clock facility;
- at least one local controller (CTR1, CTR2) associated with a processing element of the plurality of processing elements;
- a data communication means (SB) arranged for exchanging data between processing elements of the plurality of processing elements,
wherein the method comprises the following steps:
- supplying data to the processing element;
- powering down of the processing element by the local controller if no data are available for processing by the processing element;

10. A method for processing data according to claim 9, wherein the method further comprises the following step:

- powering up of the processing element by the local controller if data are available for processing by the processing element.